

IN THE CLAIMS:

Please amend the claims in the above-identified patent application as follows wherein deleted material is marked with a ~~striketrough~~ and new material is underlined to show the changes made:

1 1. (**Currently amended**) A method of extracting electrical
2 characteristics from an integrated circuit layout, said method comprising:
3 dividing said integrated circuit layout into at least one extraction sub problem;
4 identifying a set of physical parameters that define said extraction sub problem
5 from said integrated circuit layout;
6 supplying said set of physical parameters to a machine-learning model trained for
7 said extraction sub problem with Bayesian inference implemented with a
8 Monte Carlo method; and
9 calculating at least one electrical characteristic for said extraction sub problem by
10 analyzing said set of physical parameters with said machine-learning model
11 trained with Bayesian inference implemented with a Monte Carlo method.

1 2. (**Original**) The method as claimed in claim 1 wherein said electrical
2 characteristic comprises capacitance.

1 3. **(Original)** The method as claimed in claim 1 wherein said electrical
2 characteristic comprises resistance.

1 4. **(Currently amended)** The method as claimed in claim 1 wherein
2 said extraction sub problem comprises a net in said integrated circuit layout.

1 5. **(Currently amended)** The method as claimed in claim 1 wherein
2 said extraction sub problem comprises a section of interconnect wiring in said integrated
3 circuit layout.

1 6. **(Currently amended)** The method as claimed in claim 1 wherein
2 one of said set of physical parameters comprises a distance between a pair of interconnect
3 lines in said integrated circuit layout.

1 7. **(Currently amended)** The method as claimed in claim 1 wherein
2 one of said set of physical parameters comprises a an interconnect wire width in said
3 integrated circuit layout.

1 8. **(Currently amended)** The method as claimed in claim 1 wherein
2 one of said set of physical parameters comprises a an interconnect wire length in said
3 integrated circuit layout.

1 9. **(Original)** The method as claimed in claim 1, said method further
2 comprising:
3 selecting said machine-learning model from a plurality of machine-learning
4 models.

1 10. **(Currently amended)** The method as claimed in claim 1 wherein
2 calculating at least one electrical characteristic for said extraction sub problem comprises:
3 determining a capacitance per unit length for a subsection of interconnect wiring
4 in said integrated circuit layout; and
5 multiplying said capacitance per unit length by a length of said subsection of
6 interconnect wiring in said integrated circuit layout.

1 11. **(Currently amended)** A computer readable medium, said
2 computer readable medium comprising an arranged set of computer instructions for:
3 dividing an integrated circuit layout into at least one extraction sub problem;
4 identifying a set of physical parameters that define said extraction sub problem
5 from said integrated circuit layout;

6 supplying said set of physical parameters to a machine-learning model trained for
7 said extraction sub problem with Bayesian inference implemented with a
8 Monte Carlo method; and
9 calculating at least one electrical characteristic for said extraction sub problem by
10 analyzing said set of physical parameters with said machine-learning model
11 trained with Bayesian inference implemented with a Monte Carlo method.

1 12. **(Original)** The computer readable medium as claimed in claim
2 11 wherein said electrical characteristic comprises capacitance.

1 13. **(Original)** The computer readable medium as claimed in claim
2 11 wherein said electrical characteristic comprises resistance.

1 14. **(Currently amended)** The computer readable medium as claimed
2 in claim 11 wherein said extraction sub problem comprises a net in said integrated circuit
3 layout.

1 15. **(Currently amended)** The computer readable medium as claimed
2 in claim 11 wherein said extraction sub problem comprises a section of interconnect
3 wiring in said integrated circuit layout.

1 16. **(Currently amended)** The computer readable medium as claimed
2 in claim 11 wherein one of said set of physical parameters comprises a distance between a
3 pair of interconnect line in said integrated circuit layout s.

1 17. **(Currently amended)** The computer readable medium as claimed
2 in claim 11 wherein one of said set of physical parameters comprises a an interconnect
3 wire width in said integrated circuit layout.

1 18. **(Currently amended)** The method as claimed in claim ~~4~~ 11
2 wherein one of said set of physical parameters comprises a an interconnect wire length in
3 said integrated circuit layout.

1 19. **(Currently amended)** The computer readable medium as claimed
2 in claim 11 wherein said arranged set of computer instructions further perform:
3 selecting said machine-learning model trained for said extraction sub problem
4 model from a plurality of ~~extraction-sub-problem~~ machine-learning models.

1 20. (**Currently amended**) The computer readable medium as claimed
2 in claim 11 wherein a subset of computer instructions for calculating at least one
3 electrical characteristic for said extraction sub problem perform the follow:
4 determining a capacitance per unit length for a subsection of interconnect wiring
5 in said integrated circuit layout; and
6 multiplying said capacitance per unit length by a length of said subsection of
7 interconnect wiring in said integrated circuit layout.